RECEIVED
CENTRAL FAX CENTER
DEC 0 7 2004

FACSIMILE TRANSMISSION TO
THE UNITED STATES PATENT AND TRADEMARK OFFICE

DATE: 12/7/2004

RE: Serial No.: 09/932,086
Docket No.: CH00 0018

TO: Examiner: Guy Lamarre
Art Unit: 2133
Fax Number: (703) 872-9306

FROM: Michael J. Ure, Reg. No. 33,089
Telephone: (408) 474 - 9077

TRANSMISSION INCLUDES: 25 Pages (including cover sheet)
Brief for Appellant (in triplicate) – 7 pages

CERTIFICATE OF TRANSMISSION UNDER 37 CFR 1.8
I hereby certify that this correspondence is being facsimile transmitted to the Patent and Trademark Office at the number listed above
on 12/7, 2004 by
Daniel L. Michalek

PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
Intellectual Property & Standards
1109 McKay Drive M/S-41SJ
San Jose, California 95131
Fax Number: (408) 474-9082

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of FARKAS	Atty. Docket CH 000018
Serial: 09/932,086	Group Art Unit: 2133
Filed: 08/17/2001	Examiner: LAMARRE, GUY J

ARRANGEMENT FOR TESTING INTEGRATED CIRCUITS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Charge Authorization

The Commissioner is hereby requested and authorized pursuant to 37 CFR §1.136(a)(3), to treat any concurrent or future reply in this application requiring a petition for extension of time for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. Please charge any additional fees that may now or in the future be required in this application, including extension of time fees, but excluding the issue fee unless explicitly requested to do so, and credit any overpayment, to Deposit Account No. 14-1270.

BRIEF FOR APPELLANT

Sir:

Pursuant to the Notice of Appeal filed September 7, 2004, the present Brief for Appellant is submitted herewith.

REAL PARTY IN INTEREST

The real party in interest is the assignee, Philips Electronics North America Corporation.

RELATED APPEALS AND INTERFERENCES

Applicant is not aware of any related appeals or interferences.

STATUS OF CLAIMS

Claims 2, 4-5 and 10-13 are currently pending. All claims have been rejected and are on appeal.

STATUS OF AMENDMENTS

All amendments have been entered. According to the Advisory Action of 09/30/2004, the after-final amendment will be entered for purposes of appeal.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a tester and test method for testing *logic* integrated circuits (as distinguished for memory integrated circuits or analog integrated circuits, for example). Such circuits are tested using test vectors applied to external inputs of the integrated circuit or, in some instances, applied to internal inputs of the integrated circuit using scan techniques.

For complex integrated circuits, the test vectors required to achieve thorough testing may require considerable storage capacity. Refer, for example, to Fig. 1 of the specification illustrating the prior art, wherein a test system is provided with a Vector Memory 3. In another prior art approach (Fig. 2), an integrated circuit is itself provided with an on-board stimulus generator for generating test vectors and a response analyzer that analyzes the correctness of the response to generate a GO/NO-GO decision.

The present invention provides for a low-cost IC tester, illustrated in Figs. 4 and 5, that does not require a Vector Memory. The test system is provided with a stimulus generator that generates test vectors for the logic IC. In one embodiment (Fig. 4), the IC is provided with a response analyzer 5 that provides a GO/NO-GO indication to the test system. In another embodiment (Fig. 5), the response analyzer is provided within the test system itself. In this instance, since the test has access to raw test data, greater visibility into the nature of the fault may be obtained.

Claim 8 relates to a test system (2) which includes a programmable algorithmic test vector generator (4) for generating test vectors which are intended to be applied to a circuit (1) to be tested, the test system (2) being arranged to receive and evaluate test response vectors supplied by the circuit (1) to be tested.

Claim 10 relates to a tester for testing logic circuitry of an integrated circuit, comprising a programmable test vector generator for generating test vectors for the logic circuitry.

Claim 11 relates to An integrated circuit comprising means for receiving from an external tester test vectors for testing logic circuitry; and means for receiving from the logic circuitry test results in response to the test vectors, for producing a compact representation of said test results; and for outputting said compact representation to the external tester.

Claim 12 relates to a method of testing logic circuitry of an integrated circuit, comprising generating within an external tester test vectors for the logic circuitry, using a programmable test vector generator; and the integrated circuit receiving the test vectors and applying the test vectors to the logic circuitry.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Review is respectfully requested of the following grounds of rejection:

Claims 12 and 13, rejected as being anticipated by APA (Admitted Prior Art).

Claims 2, 4, and 10-13, rejected as being unpatentable over APA in view of Barry.

Claims 5, rejected as being unpatentable over APA in view of Barry further in view of Dias.

ARGUMENT

Claims 12 and 13 are Not Anticipated by APA

Considering first the rejection of claims 12 and 13, claim 12 recites in part "generating within an external tester test vectors for the logic circuitry, *using a programmable test vector generator*." Figure 1 of the specification does not illustrate any such use of a programmable test vector generator, nor does Figure 2 of the specification. Accordingly, claim 12 is not anticipated by APA. Claim 13 depends on claim 12 and therefore is also not anticipated, for like reasons.

Again in relation to claim 12, the rejection states in part "[I]t would have been obvious...to use a test vector pattern generator in an embodiment as described by Spec in Figure 1 and lines 5-10 of page 4...to prevent from having to use a large test memory as suggested by Specs in lines 10-14 of page 1." The cited passage, however, relates to test systems for *memory ICs*. There is no suggestion of the use of a programmable test vector generator for *logic circuitry* as in claim 12 and dependent claim 13.

Claims 2, 4 and 10-13 Patentably Define Over APA in View of Barry

Considering next the rejection of claims 2, 4, and 10-13, the same *non-sequitur* used in the rejection of claim 12, above, is again used in rejecting these claims. Nothing in the specification can be construed as suggesting the use of a programmable test vector generator for *logic circuitry* as in claim 10 and dependent claims 4 and 5. Similarly in relation to claim 11, there is no suggestion in the prior art of the rejection to substitute a programmable test vector generator for the vector memory of Figure 1 for the purpose of testing logic circuitry, and no motivation to combine the SISR 205 of Barry, which relates to the testing of *memory circuits*, into the *logic IC* of Figure 1.

Claim 5 Patentably Defines Over APA in View of Barry and Dias

Dias Fig. 53 shows a test vector generator 74, described as "conventional" as of the filing date of Dias (1987). There is no teaching or suggestion in Dias that the vector generator operates in real time as specified in claim 5, enabling at-speed test of the IC, for example.

CONCLUSION

For the foregoing reasons, Appellant submits that the final rejection should be REVERSED.

Respectfully submitted,

Michael J. Ure, Reg. 33,089

Dated: December 6, 2004

APPENDIX OF CLAIMS

2. The integrated circuit of claim 11, wherein the means for receiving test results comprises a test response analysis unit for compressing test response vectors, the integrated circuit further comprising a test control block for controlling the test procedure.

4. The tester of claim 10, comprising a test response analysis unit arranged to compress test response vectors received from the integrated circuit to be tested.

5. The tester of claim 10, wherein the programmable test vector generator is a programmable algorithmic test vector generator which includes an arithmetic and logic unit and generates test vectors in real time.

8. A test system (2) which includes a programmable algorithmic test vector generator (4) for generating test vectors which are intended to be applied to a circuit (1) to be tested, the test system (2) being arranged to receive and evaluate test response vectors supplied by the circuit (1) to be tested.

10. A tester for testing logic circuitry of an integrated circuit, comprising a programmable test vector generator for generating test vectors for the logic circuitry.

11. An integrated circuit comprising:

means for receiving from an external tester test vectors for testing logic circuitry; and

means for receiving from the logic circuitry test results in response to the test vectors, for producing a compact representation of said test results; and for outputting said compact representation to the external tester.

12. A method of testing logic circuitry of an integrated circuit, comprising:

generating within an external tester test vectors for the logic circuitry, using a programmable test vector generator; and

the integrated circuit receiving the test vectors and applying the test vectors to the logic circuitry.

13. The method of claim 12, wherein the integrated circuit includes a test response analysis unit, further:

receiving from the logic circuitry test results in response to the test vectors;

producing a compact representation of said test results; and

outputting said compact representation to the external tester.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of
FARKAS

Atty. Docket
CH 000018

Serial: 09/932,086

Group Art Unit: 2133

Filed: 08/17/2001

Examiner: LAMARRE, GUY J

ARRANGEMENT FOR TESTING INTEGRATED CIRCUITS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Charge Authorization

The Commissioner is hereby requested and authorized pursuant to 37 CFR §1.136(a)(3), to treat any concurrent or future reply in this application requiring a petition for extension of time for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. Please charge any additional fees that may now or in the future be required in this application, including extension of time fees, but excluding the issue fee unless explicitly requested to do so, and credit any overpayment, to Deposit Account No. 14-1270.

BRIEF FOR APPELLANT

Sir:

Pursuant to the Notice of Appeal filed September 7, 2004, the present Brief for Appellant is submitted herewith.

REAL PARTY IN INTEREST

The real party in interest is the assignee, Philips Electronics North America Corporation.

RELATED APPEALS AND INTERFERENCES

Applicant is not aware of any related appeals or interferences.

STATUS OF CLAIMS

Claims 2, 4-5 and 10-13 are currently pending. All claims have been rejected and are on appeal.

STATUS OF AMENDMENTS

All amendments have been entered. According to the Advisory Action of 09/30/2004, the after-final amendment will be entered for purposes of appeal.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a tester and test method for testing *logic* integrated circuits (as distinguished for memory integrated circuits or analog integrated circuits, for example). Such circuits are tested using test vectors applied to external inputs of the integrated circuit or, in some instances, applied to internal inputs of the integrated circuit using scan techniques.

For complex integrated circuits, the test vectors required to achieve thorough testing may require considerable storage capacity. Refer, for example, to Fig. 1 of the specification illustrating the prior art, wherein a test system is provided with a Vector Memory 3. In another prior art approach (Fig. 2), an integrated circuit is itself provided with an on-board stimulus generator for generating test vectors and a response analyzer that analyzes the correctness of the response to generate a GO/NO-GO decision.

The present invention provides for a low-cost IC tester, illustrated in Figs. 4 and 5, that does not require a Vector Memory. The test system is provided with a stimulus generator that generates test vectors for the logic IC. In one embodiment (Fig. 4), the IC is provided with a response analyzer 5 that provides a GO/NO-GO indication to the test system. In another embodiment (Fig. 5), the response analyzer is provided within the test system itself. In this instance, since the test has access to raw test data, greater visibility into the nature of the fault may be obtained.

Claim 8 relates to a test system (2) which includes a programmable algorithmic test vector generator (4) for generating test vectors which are intended to be applied to a circuit (1) to be tested, the test system (2) being arranged to receive and evaluate test response vectors supplied by the circuit (1) to be tested.

Claim 10 relates to a tester for testing logic circuitry of an integrated circuit, comprising a programmable test vector generator for generating test vectors for the logic circuitry.

Claim 11 relates to An integrated circuit comprising means for receiving from an external tester test vectors for testing logic circuitry; and means for receiving from the logic circuitry test results in response to the test vectors, for producing a compact representation of said test results; and for outputting said compact representation to the external tester.

Claim 12 relates to a method of testing logic circuitry of an integrated circuit, comprising generating within an external tester test vectors for the logic circuitry, using a programmable test vector generator; and the integrated circuit receiving the test vectors and applying the test vectors to the logic circuitry.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Review is respectfully requested of the following grounds of rejection:

Claims 12 and 13, rejected as being anticipated by APA (Admitted Prior Art).

Claims 2, 4, and 10-13, rejected as being unpatentable over APA in view of Barry.

Claims 5, rejected as being unpatentable over APA in view of Barry further in view of Dias.

ARGUMENT

Claims 12 and 13 are Not Anticipated by APA

Considering first the rejection of claims 12 and 13, claim 12 recites in part "generating within an external tester test vectors for the logic circuitry, *using a programmable test vector generator*." Figure 1 of the specification does not illustrate any such use of a programmable test vector generator, nor does Figure 2 of the specification. Accordingly, claim 12 is not anticipated by APA. Claim 13 depends on claim 12 and therefore is also not anticipated, for like reasons.

Again in relation to claim 12, the rejection states in part "[I]t would have been obvious...to use a test vector pattern generator in an embodiment as described by Spec in Figure 1 and lines 5-10 of page 4...to prevent from having to use a large test memory as suggested by Specs in lines 10-14 of page 1." The cited passage, however, relates to test systems for *memory ICs*. There is no suggestion of the use of a programmable test vector generator for *logic circuitry* as in claim 12 and dependent claim 13.

Claims 2, 4 and 10-13 Patentably Define Over APA in View of Barry

Considering next the rejection of claims 2, 4, and 10-13, the same *non-sequitur* used in the rejection of claim 12, above, is again used in rejecting these claims. Nothing in the specification can be construed as suggesting the use of a programmable test vector generator for *logic circuitry* as in claim 10 and dependent claims 4 and 5. Similarly in relation to claim 11, there is no suggestion in the prior art of the rejection to substitute a programmable test vector generator for the vector memory of Figure 1 for the purpose of testing logic circuitry, and no motivation to combine the SISR 205 of Barry, which relates to the testing of *memory circuits*, into the *logic IC* of Figure 1.

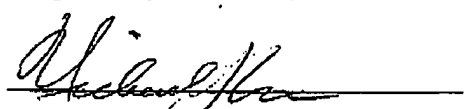
Claim 5 Patentably Defines Over APA in View of Barry and Dias

Dias Fig. 53 shows a test vector generator 74, described as "conventional" as of the filing date of Dias (1987). There is no teaching or suggestion in Dias that the vector generator operates in real time as specified in claim 5, enabling at-speed test of the IC, for example.

CONCLUSION

For the foregoing reasons, Appellant submits that the final rejection should be REVERSED.

Respectfully submitted,



Michael J. Ure, Reg. 33,089

Dated: December 6, 2004

APPENDIX OF CLAIMS

2. The integrated circuit of claim 11, wherein the means for receiving test results comprises a test response analysis unit for compressing test response vectors, the integrated circuit further comprising a test control block for controlling the test procedure.

4. The tester of claim 10, comprising a test response analysis unit arranged to compress test response vectors received from the integrated circuit to be tested.

5. The tester of claim 10, wherein the programmable test vector generator is a programmable algorithmic test vector generator which includes an arithmetic and logic unit and generates test vectors in real time.

8. A test system (2) which includes a programmable algorithmic test vector generator (4) for generating test vectors which are intended to be applied to a circuit (1) to be tested, the test system (2) being arranged to receive and evaluate test response vectors supplied by the circuit (1) to be tested.

10. A tester for testing logic circuitry of an integrated circuit, comprising a programmable test vector generator for generating test vectors for the logic circuitry.

11. An integrated circuit comprising:

means for receiving from an external tester test vectors for testing logic circuitry; and

means for receiving from the logic circuitry test results in response to the test vectors, for producing a compact representation of said test results; and for outputting said compact representation to the external tester.

12. A method of testing logic circuitry of an integrated circuit, comprising:

generating within an external tester test vectors for the logic circuitry, using a programmable test vector generator; and

the integrated circuit receiving the test vectors and applying the test vectors to the logic circuitry.

13. The method of claim 12, wherein the integrated circuit includes a test response analysis unit, further:

receiving from the logic circuitry test results in response to the test vectors;

producing a compact representation of said test results; and

outputting said compact representation to the external tester.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of FARKAS	Atty. Docket CH 000018
Serial: 09/932,086	Group Art Unit: 2133
Filed: 08/17/2001	Examiner: LAMARRE, GUY J

ARRANGEMENT FOR TESTING INTEGRATED CIRCUITS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Charge Authorization

The Commissioner is hereby requested and authorized pursuant to 37 CFR §1.136(a)(3), to treat any concurrent or future reply in this application requiring a petition for extension of time for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. Please charge any additional fees that may now or in the future be required in this application, including extension of time fees, but excluding the issue fee unless explicitly requested to do so, and credit any overpayment, to Deposit Account No. 14-1270.

BRIEF FOR APPELLANT

Sir:

Pursuant to the Notice of Appeal filed September 7, 2004, the present Brief for Appellant is submitted herewith.

REAL PARTY IN INTEREST

The real party in interest is the assignee, Philips Electronics North America Corporation.

RELATED APPEALS AND INTERFERENCES

Applicant is not aware of any related appeals or interferences.

STATUS OF CLAIMS

Claims 2, 4-5 and 10-13 are currently pending. All claims have been rejected and are on appeal.

STATUS OF AMENDMENTS

All amendments have been entered. According to the Advisory Action of 09/30/2004, the after-final amendment will be entered for purposes of appeal.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a tester and test method for testing *logic* integrated circuits (as distinguished for memory integrated circuits or analog integrated circuits, for example). Such circuits are tested using test vectors applied to external inputs of the integrated circuit or, in some instances, applied to internal inputs of the integrated circuit using scan techniques.

For complex integrated circuits, the test vectors required to achieve thorough testing may require considerable storage capacity. Refer, for example, to Fig. 1 of the specification illustrating the prior art, wherein a test system is provided with a Vector Memory 3. In another prior art approach (Fig. 2), an integrated circuit is itself provided with an on-board stimulus generator for generating test vectors and a response analyzer that analyzes the correctness of the response to generate a GO/NO-GO decision.

The present invention provides for a low-cost IC tester, illustrated in Figs. 4 and 5, that does not require a Vector Memory. The test system is provided with a stimulus generator that generates test vectors for the logic IC. In one embodiment (Fig. 4), the IC is provided with a response analyzer 5 that provides a GO/NO-GO indication to the test system. In another embodiment (Fig. 5), the response analyzer is provided within the test system itself. In this instance, since the test has access to raw test data, greater visibility into the nature of the fault may be obtained.

Claim 8 relates to a test system (2) which includes a programmable algorithmic test vector generator (4) for generating test vectors which are intended to be applied to a circuit (1) to be tested, the test system (2) being arranged to receive and evaluate test response vectors supplied by the circuit (1) to be tested.

Claim 10 relates to a tester for testing logic circuitry of an integrated circuit, comprising a programmable test vector generator for generating test vectors for the logic circuitry.

Claim 11 relates to An integrated circuit comprising means for receiving from an external tester test vectors for testing logic circuitry; and means for receiving from the logic circuitry test results in response to the test vectors, for producing a compact representation of said test results; and for outputting said compact representation to the external tester.

Claim 12 relates to a method of testing logic circuitry of an integrated circuit, comprising generating within an external tester test vectors for the logic circuitry, using a programmable test vector generator; and the integrated circuit receiving the test vectors and applying the test vectors to the logic circuitry.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Review is respectfully requested of the following grounds of rejection:

Claims 12 and 13, rejected as being anticipated by APA (Admitted Prior Art).

Claims 2, 4, and 10-13, rejected as being unpatentable over APA in view of Barry.

Claims 5, rejected as being unpatentable over APA in view of Barry further in view of Dias.

ARGUMENT

Claims 12 and 13 are Not Anticipated by APA

Considering first the rejection of claims 12 and 13, claim 12 recites in part "generating within an external tester test vectors for the logic circuitry, *using a programmable test vector generator.*" Figure 1 of the specification does not illustrate any such use of a programmable test vector generator, nor does Figure 2 of the specification. Accordingly, claim 12 is not anticipated by APA. Claim 13 depends on claim 12 and therefore is also not anticipated, for like reasons.

Again in relation to claim 12, the rejection states in part "[I]t would have been obvious...to use a test vector pattern generator in an embodiment as described by Spec in Figure 1 and lines 5-10 of page 4...to prevent from having to use a large test memory as suggested by Specs in lines 10-14 of page 1." The cited passage, however, relates to test systems for *memory ICs*. There is no suggestion of the use of a programmable test vector generator for *logic circuitry* as in claim 12 and dependent claim 13.

Claims 2, 4 and 10-13 Patentably Define Over APA in View of Barry

Considering next the rejection of claims 2, 4, and 10-13, the same *non-sequitur* used in the rejection of claim 12, above, is again used in rejecting these claims. Nothing in the specification can be construed as suggesting the use of a programmable test vector generator for *logic circuitry* as in claim 10 and dependent claims 4 and 5. Similarly in relation to claim 11, there is no suggestion in the prior art of the rejection to substitute a programmable test vector generator for the vector memory of Figure 1 for the purpose of testing logic circuitry, and no motivation to combine the SISR 205 of Barry, which relates to the testing of *memory circuits*, into the *logic IC* of Figure 1.

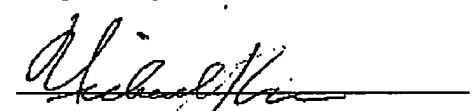
Claim 5 Patentably Defines Over APA in View of Barry and Dias

Dias Fig. 53 shows a test vector generator 74, described as "conventional" as of the filing date of Dias (1987). There is no teaching or suggestion in Dias that the vector generator operates in real time as specified in claim 5, enabling at-speed test of the IC, for example.

CONCLUSION

For the foregoing reasons, Appellant submits that the final rejection should be REVERSED.

Respectfully submitted,



Michael J. Ure, Reg. 33,089

Dated: December 6, 2004

APPENDIX OF CLAIMS

2. The integrated circuit of claim 11, wherein the means for receiving test results comprises a test response analysis unit for compressing test response vectors, the integrated circuit further comprising a test control block for controlling the test procedure.

4. The tester of claim 10, comprising a test response analysis unit arranged to compress test response vectors received from the integrated circuit to be tested.

5. The tester of claim 10, wherein the programmable test vector generator is a programmable algorithmic test vector generator which includes an arithmetic and logic unit and generates test vectors in real time.

8. A test system (2) which includes a programmable algorithmic test vector generator (4) for generating test vectors which are intended to be applied to a circuit (1) to be tested, the test system (2) being arranged to receive and evaluate test response vectors supplied by the circuit (1) to be tested.

10. A tester for testing logic circuitry of an integrated circuit, comprising a programmable test vector generator for generating test vectors for the logic circuitry.

11. An integrated circuit comprising:

means for receiving from an external tester test vectors for testing logic circuitry; and

means for receiving from the logic circuitry test results in response to the test vectors, for producing a compact representation of said test results; and for outputting said compact representation to the external tester.

12. A method of testing logic circuitry of an integrated circuit, comprising:

generating within an external tester test vectors for the logic circuitry, using a programmable test vector generator; and

the integrated circuit receiving the test vectors and applying the test vectors to the logic circuitry.

13. The method of claim 12, wherein the integrated circuit includes a test response analysis unit, further:

receiving from the logic circuitry test results in response to the test vectors;

producing a compact representation of said test results; and

outputting said compact representation to the external tester.